Mixed Voltage VLSI Design

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Abstract

Low voltage operation in VLSI leads to slower circuits which can result in a lower system throughput. However, the throughput of a VLSI chip is determined by the speed of its critical path(s) and the gates that are not in the critical path(s) can be slowed down without affecting the overall chip throughput. This paper investigates the design of VLSI chips with two voltage levels to ensure lower power without sacrificing the overall chip throughput.

Summary

The thrust towards less power-hungry VLSI chips is motivated by the dual considerations of prolonging battery operation and cooling future 3D VLSI systems. One of the ways of achieving lower power in VLSI is to reduce the operating voltage for the chip since the power consumed is proportional to the square of the operating voltage. Thus, 3.3V operation instead of 5V operation results in 56% reduction in the power consumption of a chip. However, low voltage operation also exacts a penalty in the speed of the circuits which results in lower chip throughput. The overall chip throughput is determined by the speed of the critical path(s) in the chip. The gates that are not in the critical path(s) can be operated at the lower voltage while the gates in the critical path(s) are operated at the higher voltage. This technique of mixed voltage design results in chips that consume significantly less power without affecting the overall chip throughput. We present some of the issues involved in mixed voltage design that we have considered for three VLSI chips that were designed at JPL for various flight projects. We present data on the designs of these chips and show the power savings that can result from a mixed voltage design. The designs of the chips have a bimodal distribution of path lengths with the majority (typically 90%) of the paths capable of slower operation. However, some sections of the shorter paths intersect with the longer paths and hence some critical sections of the shorter paths may need to be operated at the higher voltage to ensure that the speed of the longer critical path(s) is not compromised. The interface between the gates which operate at different voltages is an important issue which needs close attention because of the possibility of increased static currents at the interface. We show how the interface between the two voltage levels can be accomplished by transistor sizing. Spice simulations show that transistor sizing allows the interface to be accomplished without any significant static current dissipation. We then present a greedy algorithm for determining the gates which can be operated at the lower voltage. The input to the algorithm is an adjacency list representation of the chip which is extracted from the design netlist. The algorithm is fast and produces results that are close to optimal. Finally, we present results on the performance of the algorithm for the three chip designs.